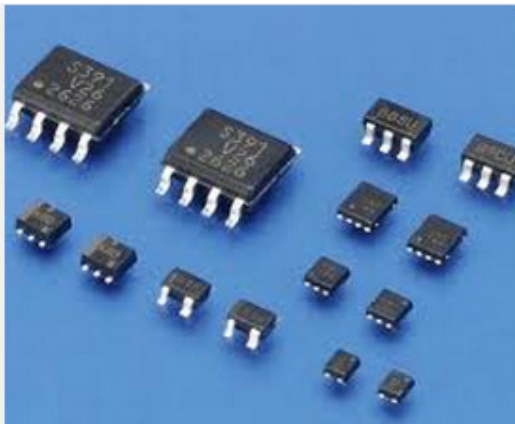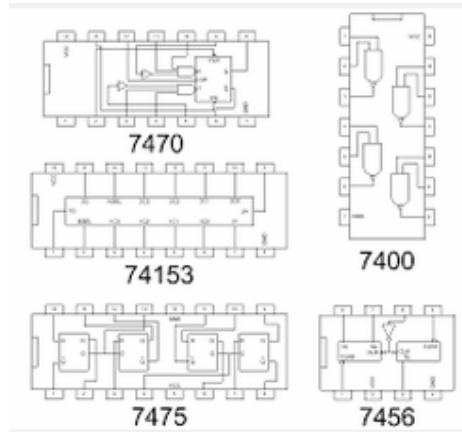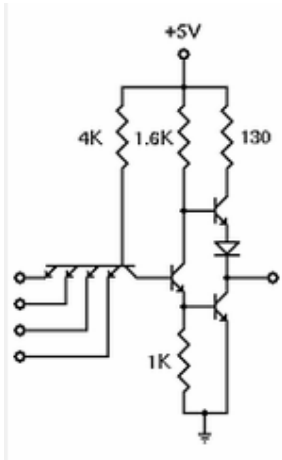**Transistor–transistor logic** (**TTL**) is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. It is called *transistor–transistor logic* because both the logic gating function (e.g.,AND) and the amplifying function are performed by transistors (contrast with RTL and DTL).

TTL is notable for being a widespread integrated circuit (IC) family used in many applications such as computers, industrial controls, test equipment and instrumentation, consumer electronics, synthesizers, etc. The designation *TTL* is sometimes used to mean TTL-compatible logic levels, even when not associated directly with TTL integrated circuits, for example as a label on the inputs and outputs of electronic instruments.[1]

After their introduction in integrated circuit form in 1963 by Sylvania, TTL integrated circuits were manufactured by several semiconductor companies, with the 7400 series by Texas

Instruments becoming particularly popular. TTL manufacturers offered a wide range of logic gate, flip-flops, counters, and other circuits. Several variations from the original bipolar TTL concept were developed, giving circuits with higher speed or lower power dissipation to allow optimization of a design. TTL circuits simplified design of systems compared to earlier logic families, offering superior speed to resistor–transistor logic (RTL) and easier design layout than emitter-coupled logic(ECL). The design of the input and outputs of TTL gates allowed many elements to be interconnected.

TTL became the foundation of computers and other digital electronics. Even after much larger scale integrated circuits made multiple-circuit-board processors obsolete, TTL devices still found extensive use as the "glue" logic interfacing more densely integrated components. TTL devices were originally made in ceramic and plastic dual-in-line (DIP) packages, and flat-pack form. TTL chips are now also made in surface-mount packages. Successors to the original bipolar TTL logic often are interchangeable in function with the original circuits, but with improved speed or lower power dissipation.

History

A real-time clock built of TTL chips around 1979.

TTL was invented in 1961 by James L. Buie of TRW, "particularly suited to the newly developing integrated circuit design technology", and it was originally named *transistor-coupled transistor logic* (TCTL).[2]The first commercial integrated-circuit TTL devices were manufactured by Sylvania in 1963, called the Sylvania Universal High-Level Logic family (SUHL).[3] The Sylvania parts were used in the controls of the Phoenix missile.[3] TTL became popular with electronic systems designers after Texas Instruments introduced the 5400 series of ICs, with military temperature range, in 1964 and the later 7400 series, specified over a narrower range, and with inexpensive plastic packages in 1966.[4]

The Texas Instruments 7400 family became an industry standard. Compatible parts were made by Motorola, AMD, Fairchild, Intel, Intersil,Signetics, Mullard, Siemens, SGS-Thomson and National Semiconductor,[5][6] and many other companies, even in the Eastern Bloc (Soviet Union, GDR, Poland,

Bulgaria).[citation needed] Not only did others make compatible TTL parts, but compatible parts were made using many other circuit technologies as well. At least one manufacturer, IBM, produced non-compatible TTL circuits for its own use; IBM used the technology in the IBM System/38, IBM 4300, and IBM 3081.[7]

The term "TTL" is applied to many successive generations of bipolar logic, with gradual improvements in speed and power consumption over about two decades. The most recently introduced family[citation needed], 74AS/ALS Advanced Schottky, was introduced in 1985.[8] As of 2008, Texas Instruments continues to supply the more general-purpose chips in numerous obsolete technology families, albeit at increased prices. Typically, TTL chips integrate no more than a few hundred transistors each. Functions within a single package generally range from a few logic gates to a microprocessor bit-slice. TTL also became important because its low cost made digital techniques economically practical for tasks previously done by analog methods.[9]

Introduction to Digital Logic Gates

A Digital Logic Gate is an electronic device that makes logical decisions based on the different combinations of digital signals present on its inputs. Digital logic gates may have more than one input but generally only have one digital output. Individual logic gates can be connected together to form combinational or sequential circuits, or larger logic gate functions.

Standard commercially available digital logic gates are available in two basic families or forms, **TTL** which stands for *Transistor-Transistor Logic* such as the 7400 series, and **CMOS** which stands for *Complementary Metal-Oxide-Silicon* which is the 4000 series of chips. This notation of TTL or CMOS refers to the logic technology used to manufacture the integrated circuit, (IC) or a "chip" as it is more commonly called.

Digital Logic Gate

Generally speaking, **TTL** logic IC's use NPN and PNP type **Bipolar Junction Transistors** while **CMOS** logic IC's use complementary MOSFET or JFET type **Field Effect Transistors** for both their input and output circuitry.

As well as TTL and CMOS technology, simple Digital Logic Gates can also be made by connecting together diodes, transistors and resistors to produce **RTL**, Resistor-Transistor logic gates, **DTL**, Diode-Transistor logic gates or **ECL**, Emitter-Coupled logic gates but these are less common now compared to the popular **CMOS** family.

Integrated Circuits or IC's as they are more commonly called, can be grouped together into families according to the number of transistors or "gates" that they contain. For example, a simple AND gate my contain only a few individual transistors, were as a more complex microprocessor may contain many thousands of individual transistor gates. Integrated circuits are categorised according to the number of logic gates or the complexity of the circuits within a single chip with the general classification for the number of individual gates given as:

- Small Scale Integration or (SSI) – Contain up to 10 transistors or a few gates within a single package such as AND, OR, NOT gates.

- Medium Scale Integration or (MSI) – between 10 and 100 transistors or tens of gates within a single package and perform digital operations such as adders, decoders, counters, flip-flops and multiplexers.

- Large Scale Integration or (LSI) – between 100 and 1,000 transistors or hundreds of gates and perform specific digital operations such as I/O chips, memory, arithmetic and logic units.

- Very-Large Scale Integration or (VLSI) – between 1,000 and 10,000 transistors or thousands of gates and perform computational operations such as processors, large memory arrays and programmable logic devices.

- Super-Large Scale Integration or (SLSI) – between 10,000 and 100,000 transistors within a single package and perform computational operations such as microprocessor chips, micro-controllers, basic PICs and calculators.

- Ultra-Large Scale Integration or (ULSI) – more than 1 million transistors – the big boys that are used in computers CPUs, GPUs, video processors, micro-controllers, FPGAs and complex PICs.

While the "ultra large scale" ULSI classification is less well used, another level of integration which represents the complexity of the Integrated Circuit is known as the **System-on-Chip** or (**SOC**) for short. Here the individual components such as the microprocessor, memory, peripherals, I/O logic etc, are all produced on a single piece of silicon and which represents a whole electronic system within one single chip, literally putting the word "integrated" into integrated circuit.

These complete integrated chips which can contain up to 100 million individual silicon-CMOS transistor gates within one single package are generally used in mobile phones, digital cameras, micro-controllers, PIC's and robotic type applications.

Moore's Law

In 1965, Gordon Moore co-founder of the Intel corporation predicted that "*The number of transistors and resistors on a single chip will double every 18 months*" regarding the development of semiconductor gate technology. When Gordon Moore made his famous comment way back in 1965 there were approximately only 60 individual transistor gates on a single silicon chip or die.

The worlds first microprocessor in 1971 was the Intel 4004 that had a 4-bit data bus and contained about 2,300 transistors on a single chip, operating at about 600kHz. Today, the Intel Corporation have placed a staggering 1.2 Billion individual transistor gates onto its new Quad-core i7-2700K Sandy Bridge 64-bit microprocessor chip operating at nearly 4GHz, and the on-chip transistor count is still rising, as newer faster microprocessors and micro-controllers are developed.

Digital Logic States

The **Digital Logic Gate** is the basic building block from which all digital electronic circuits and microprocessor based systems are constructed from. Basic digital logic gates perform logical operations of AND, OR and NOT on binary numbers.

In digital logic design only two voltage levels or states are allowed and these states are generally referred to as Logic "1" and Logic "0", High and Low, or True and False. These two states are represented in **Boolean Algebra** and standard truth tables by the binary digits of "1" and "0" respectively.

A good example of a digital state is a simple light switch as it is either "ON" or "OFF" but not both at the same time. Then we can summarise the relationship between these various digital states as being:

Boolean Algebra	Boolean Logic	Voltage State
Logic "1"	True (T)	High (H)
Logic "0"	False (F)	Low (L)

Most *digital logic gates* and digital logic systems use "Positive logic", in which a logic level "0" or "LOW" is represented by a zero voltage, 0v or ground and a logic level "1" or "HIGH" is represented by a higher voltage such as +5 volts, with the switching from one voltage level to the other, from either a logic level "0" to a "1" or a "1" to a "0" being made as quickly as possible to prevent any faulty operation of the logic circuit.

There also exists a complementary "Negative Logic" system in which the values and the rules of a logic "0" and a logic "1" are reversed but in this tutorial section about digital logic gates we shall only refer to the positive logic convention as it is the most commonly used.

In standard TTL (transistor-transistor logic) IC's there is a pre-defined voltage range for the input and output voltage levels which define exactly what is a logic "1" level and what is a logic "0" level and these are shown below.

TTL Input & Output Voltage Levels
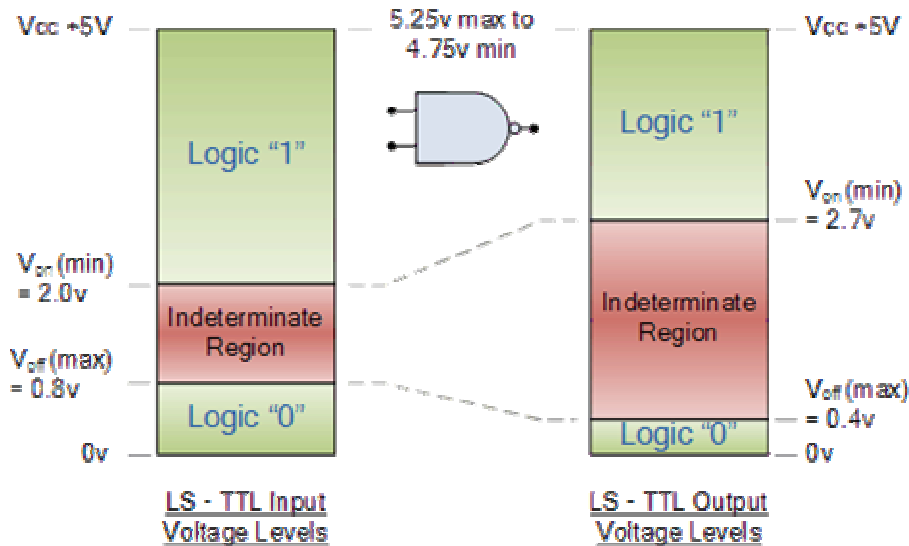
There are a large variety of logic gate types in both the bipolar 7400 and the CMOS 4000 families of digital logic gates such as 74Lxx, 74LSxx, 74ALSxx, 74HCxx, 74HCTxx, 74ACTxx etc, with each one having its own distinct advantages and disadvantages compared to the other. The exact switching voltage required to produce either a logic "0" or a logic "1" depends upon the specific logic group or family.

However, when using a standard +5 volt supply any TTL voltage input between 2.0v and 5v is considered to be a logic "1" or "HIGH" while any voltage input below 0.8v is recognised as a logic "0" or

"LOW". The voltage region in between these two voltage levels either as an input or as an output is called the *Indeterminate Region* and operating within this region may cause the logic gate to produce a false output.

The CMOS 4000 logic family uses different levels of voltages compared to the TTL types as they are designed using field effect transistors, or FET's. In CMOS technology a logic "1" level operates between 3.0 and 18 volts and a logic "0" level is below 1.5 volts. Then the following table shows the difference between the logic levels of traditional TTL and CMOS logic gates.

TTL and CMOS Logic Levels

Device Type	Logic 0	Logic 1
TTL	0 to 0.8v	2.0 to 5v (V_{cc})
CMOS	0 to 1.5v	3.0 to 18v (V_{DD})

Then from the above observations, we can define the ideal TTL digital logic gate as one that has a "LOW" level logic "0" of 0 volts (ground) and a "HIGH" level logic "1" of +5 volts and this can be demonstrated as:

Ideal TTL Digital Logic Gate Voltage Levels
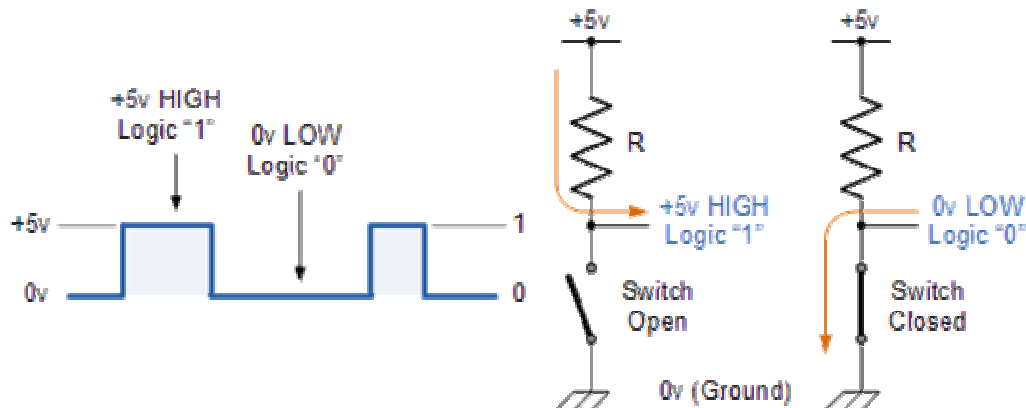
Where the opening or closing of the switch produces either a logic level "1" or a logic level "0" with the resistor R being known as a "pull-up" resistor.

Digital Logic Noise

However, between these defined HIGH and LOW values lies what is generally called a "no-man's land" (the blue area's above) and if we apply a signal voltage of a value within this no-man's land area we do not know whether the logic gate will respond to it as a level "0" or as a level "1", and the output will become unpredictable.

Noise is the name given to a random and unwanted voltage that is induced into electronic circuits by external interference, such as from nearby switches, power supply fluctuations or from wires and other conductors that pick-up stray electromagnetic radiation. Then in order for a logic gate not to be influence by noise in must have a certain amount of noise margin or noise immunity.
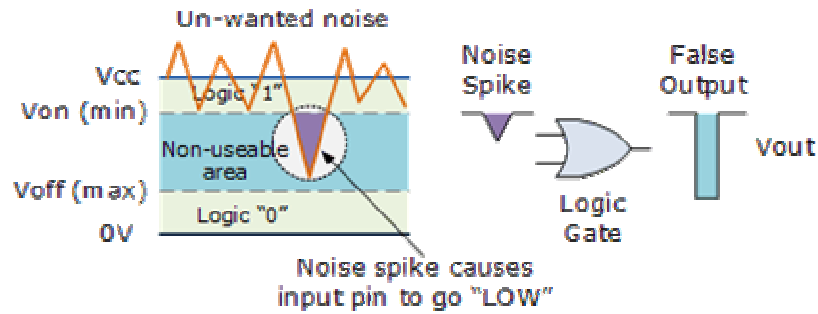
In the example above, the noise signal is superimposed onto the Vcc supply voltage and as long as it stays above the minimum level (Von-min) the input an corresponding output of the logic gate are unaffected. But when the noise level becomes large enough and a noise spike causes the HIGH voltage level to drop below this minimum level, the logic gate may interpret this spike as a LOW level input and switch the output accordingly producing a false output switching. Then in order for the logic gate not to be affected by noise it must be able to tolerate a certain amount of unwanted noise on its input without changing the state of its output.

Simple Basic Digital Logic Gates

Simple digital logic gates can be made by combining transistors, diodes and resistors with a simple example of a Diode-Resistor Logic (DRL) AND gate and a Diode-Transistor Logic (DTL) NAND gate given below.
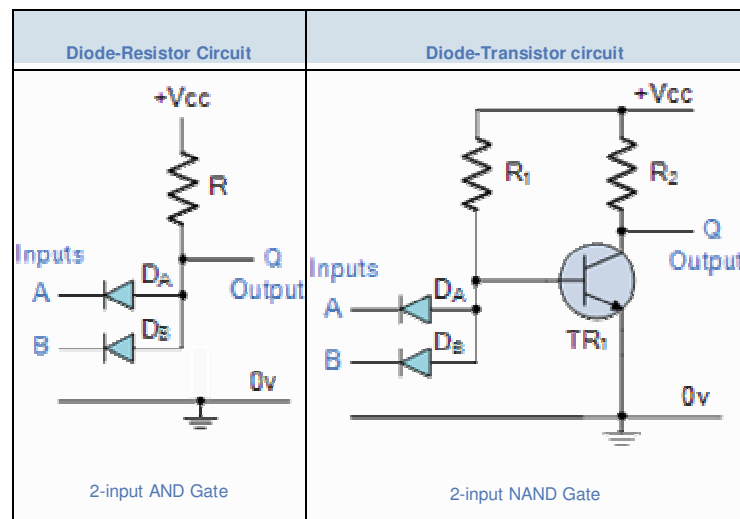

The simple 2-input Diode-Resistor AND gate can be converted into a NAND gate by the addition of a single transistor inverting (NOT) stage. Using discrete components such as diodes, resistors and transistors to make digital logic gate circuits are not used in practical commercially available logic IC's as these circuits suffer from propagation delay or gate delay and also power loss due to the pull-up resistors.

Another disadvantage of diode-resistor logic is that there is no "Fan-out" facility which is the ability of a single output to drive many inputs of the next stages. Also this type of design does not turn fully "OFF" as a Logic "0" produces an output voltage of 0.6v (diode voltage drop), so the following TTL and CMOS circuit designs are used instead.

The simple Diode-Resistor AND gate above uses separate diodes for its inputs, one for each input. As a transistor is made up off two diode circuits connected together representing an NPN or a PNP device, the input diodes of the DTL circuit can be replaced by one single NPN transistor with multiple emitter inputs as shown.
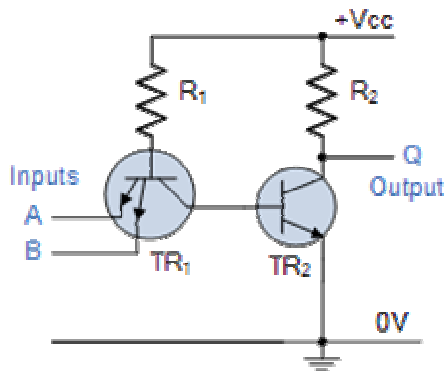
2-input NAND Gate

As the NAND gate contains a single stage inverting NPN transistor circuit (TR_2) an output logic level "1" at Q is only present when both the emitters of TR_1 are connected to logic level "0" or ground allowing base current to pass through the PN junctions of the emitter and not the collector. The multiple emitters of TR_1 are connected as inputs thus producing a NAND gate function.

In standard TTL logic gates, the transistors operate either completely in the "cut off" region, or else completely in the saturated region, **Transistor as a Switch** type operation.

Emitter-Coupled Digital Logic Gate

Emitter Coupled Logic or **ECL** is another type of digital logic gate that uses bipolar transistor logic where the transistors are not operated in the saturation region, as they are with the standard TTL digital logic gate. Instead the input and output circuits are push-pull connected transistors with the supply voltage negative with respect to ground.

This has the effect of increasing the speed of operation of the emitter coupled logic gates up to the Gigahertz range compared with the standard TTL types, but noise has a greater effect in ECL logic, because the unsaturated transistors operate within their active region and amplify as well as switch signals.

The "74" Sub-families of Integrated Circuits

With improvements in the circuit design to take account of propagation delays, current consumption, fan-in and fan-out requirements etc, this type of TTL bipolar transistor technology forms the basis of the prefixed "74" family of digital logic IC's, such as the "7400" Quad 2-input ANDgate, or the "7402" Quad 2-input OR gate, etc.

Sub-families of the 74xx series IC's are available relating to the different technologies used to fabricate the gates and they are denoted by the letters in between the 74 designation and the device number. There are a number of TTL sub-families available that provide a wide range of switching speeds and power consumption such as the 74**L**00 or 74**ALS**00 AND gate, were the "L" stands for "Low-power TTL" and the "ALS" stands for "Advanced Low-power Schottky TTL" and these are listed below.

Basic CMOS Digital Logic Gate

One of the main disadvantages with the TTL digital logic gate series is that the logic gates are based on bipolar transistor logic technology and as transistors are current operated devices, they consume large amounts of power from a fixed +5 volt power supply.

Also, TTL bipolar transistor gates have a limited operating speed when switching from an "OFF" state to an "ON" state and vice-versa called the "gate" or "propagation delay". To overcome these limitations complementary MOS called "CMOS" (**C**omplementary **M**etal **O**xide **S**emiconductor) logic gates which use "Field Effect Transistors" or FET's were developed.

As these gates use both P-channel and N-channel MOSFET's as their input device, at quiescent conditions with no switching, the power consumption of CMOS gates is almost zero, (1 to 2uA) making them ideal for use in low-power battery circuits and with switching speeds upwards of 100MHz for use in high frequency timing and computer circuits.
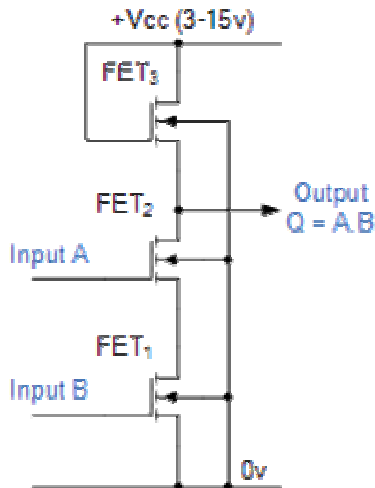
2-input NAND Gate

This CMOS gate example contains 3 N-channel MOSFET's, one for each input FET_1 and FET_2 and one for the output FET_3. When both the inputs A and B are at logic level "0", FET_1 and FET_2 are both switched "OFF" giving an output logic "1" from the source of FET_3.

When one or both of the inputs are at logic level "1" current flows through the corresponding FET giving an output state at Q equivalent to logic "0", thus producing a NAND gate function.

Improvements in the circuit design with regards to switching speed, low power consumption and improved propagation delays has resulted in the standard CMOS 4000 "CD" family of logic IC's being developed that complement the TTL range.

As with the standard TTL digital logic gates, all the major digital logic gates and devices are available in the CMOS package such as the CD4011, a Quad 2-input NAND gate, or the CD4001, a Quad 2-input NOR gate along with all their sub-families.

Like TTL logic, complementary MOS (CMOS) circuits take advantage of the fact that both N-channel and P-channel devices can be fabricated together on the same substrate material to form various logic functions.

One of the main disadvantage with the CMOS range of IC's compared to their equivalent TTL types is that they are easily damaged by static electricity. Also unlike TTL logic gates that operate on single +5V voltages for both their input and output levels, CMOS digital logic gates operate on a single supply voltage of between +3 and +18 volts.

Common CMOS Sub-families include:

- • 4000B Series: Standard CMOS – These devices are the original Buffered CMOS family of logic gates introduced in the early 70's and operate from a supply voltage of 3.0 to 18v d.c.

- • 74C Series: 5v CMOS – These devices are pin-compatible with standard 5v TTL devices as their logic switching is implemented in CMOS but with TTL-compatible inputs. They operate from a supply voltage of 3.0 to 18v d.c.

Note that CMOS logic gates and devices are static sensitive, so always take the appropriate precautions of working on antistatic mats or grounded workbenches, wearing an antistatic wristband and not removing a part from its antistatic packaging until required.

In the next tutorial about **Digital Logic Gates**, we will look at the digital Logic **AND Gate** function as used in both TTL and CMOS logic circuits as well as its Boolean Algebra definition and truth tables.
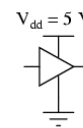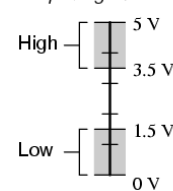
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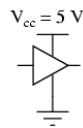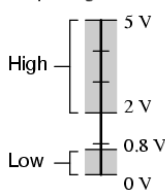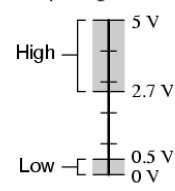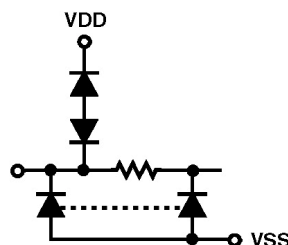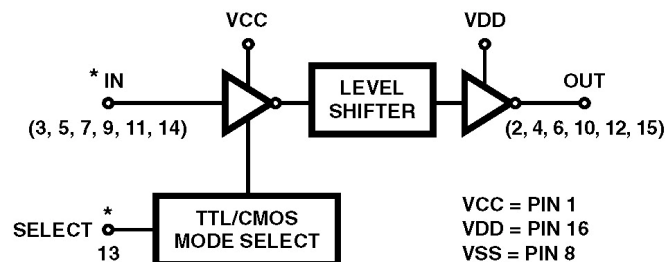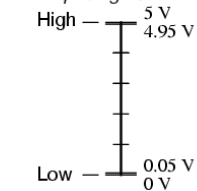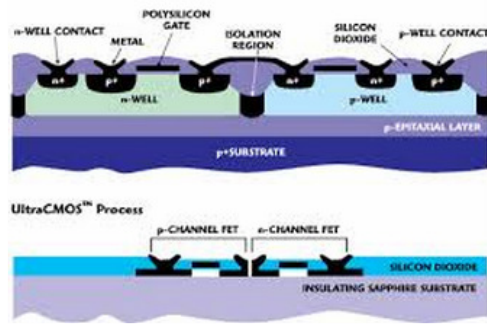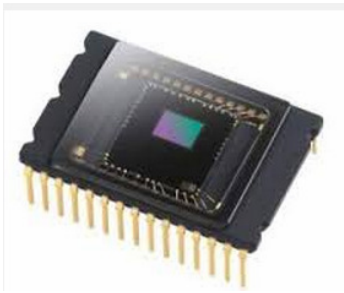
CMOS Technology

Written By:

Preeti Jain

The first working point contact transistor developed by John Bardeen, Walter Brattain and William Shockley at Bell laboratories in 1947 initiated the rapid growth of the information technology industry. In 1958, J Kilby invented the first integrated circuit flip flop at Texas and soon after this; Frank Wanlass at Fairchild described the first CMOS logic gate (nMOS and pMOS) in 1963.

The most common description of the evolution of CMOS technology is known as Moore's law. In 1963 Gordon Moore predicted that as a result of continuous miniaturization, transistor count would double every 18 months. The observation made by Gordon Moore was that the number of components on the most complex integrated circuit chip would double each year for the next 10 years. This doubling was based on a 50 – 60-component chip produced at that point of time compared with those produced in preceding years. Looks surprising, but his prediction has turned true and is being treated as a law. The speed of transistors increases and their cost decreases as their size is reduced. The transistors manufactured today are 20 times faster and occupy less than 1% of the area of those built 20-30 years ago. In 1971, Intel 4004 had transistors with minimum dimension of 10um and in 2003; Pentium 4 had transistors with minimum dimension of 130 nm. Having crossed 90nm, 65nm technological nodes, 32 nm and 22nm technology is in the pipeline. 53% compound annual growth rate is achieved over 45 years. No other technology has grown so fast so long. Transistors have become smaller, faster, consume less power, and are cheaper to manufacture. It seems intuitively obvious that scaling cannot go on forever because transistors cannot be smaller than atoms.

The first integrated circuits hitting the markets in the seventies had a few **100** transistors integrated in bipolar technology. Even though the principles were well known, MOS arrived in the markets several years later. One of the reasons behind this was the inherent instability of the MOS transistors due to the presence of minute amounts of alkali elements in the gate dielectric. This caused the threshold voltage of the transistor to shift during the operation.

However, soon the problems of high power consumption by bipolar circuits became dominant. Even in the case of all transistors being 'OFF', the sum of the leakage current in bipolar transistors is fairly large. To provide a solution for the problem of power consumption, **MOS** technology eventually made its way. Dimensions of MOS devices can be scaled down more easily than other transistor types.

In principle, MOS is better in terms of power consumption. MOS devices work with only switching voltages; current per se is not needed for the operation. MOS circuits do have lower power consumption; but they are also slower than their bipolar colleagues. Initially, NMOS got wider acceptance but with the increase in integration density, power consumption again became a problem. Afterwards, in eighties, CMOS processes were widely adopted. Present day chips would not exist if the CMOS technique would not have been implemented around the late eighties.

IC TECHNOLOGIES

Silicon IC technologies can be primarily classified under three types:

{C·   Bipolar

Bipolar transistors have npn or pnp silicon structure. In these transistors, small current into very thin base layer controls large currents between emitter and collector. Base currents limit integration density of bipolar devices.

{C}·   Metal Oxide Semiconductor(MOS)

MOS is further classified under PMOS (P-type MOS), NMOS (N-type MOS) and CMOS (Complementary MOS). MOS derives its name from the basic physical structure of these devices; MOS devices comprise of a semiconductor, oxide and a metal gate. Nowadays, polySi is more widely used as gate. Voltage applied to the gate controls the current between source and drain. Since they consume very low power, MOS allows very high integration.

{C·   BiCMOS(Bipolar CMOS technology)

BiCMOS Technology utilizes both CMOS and Bipolar Junction transistors integrated on the same semiconductor chip.

CMOS offers high, symmetrical noise margins, high input and low output impedance, high packing density, and low power dissipation but speed is the only restricting factor. In contrast, the ECL gate has a high current drive per unit area, high switching speed, smaller propagation delay, but high power consumption makes very large scale integration difficult.

BiCMOS has made it possible to combine CMOS transistors and bipolar devices in a single process at a reasonable cost to achieve the high-density integration of MOS logic with the current-driving capabilities of bipolar transistors.

Some other variants of FETs have also come up, viz., Si-TFT, polySi-TFT, MESFET, etc. These are used for different applications.